REMARKS

Claims 1-25 are pending in the application. Claims 1 and 25 have been amended by the present amendment. The amendment is fully supported by the specification as originally filed (see, e.g., page 34, line 23 to page 35, line 6).

Claims 1 and 25 have been amended to clarify that the transfer gate of a corresponding register block is brought into an ON-state **only** when there is a **change** of output of the flip-flop of the corresponding register block.

For example, with reference to FIGS. 1, 2C, and 2D of the application, the transfer gate TG1 is brought into an ON-state only in a specified period during which the output OUT1 of the flip-flop FF1 changes (see, e.g., specification at page 35, lines 4-6). Referring to FIGS. 2C and 2D, "CTL1" represents a control signal for turning ON the transfer gate TG1 (see FIG. 2C), and "OUT1" represents an output of the flip-flop FF1. As shown in FIGS. 2C and 2D, the transfer gate is ON (see steps in FIG. 2C) only when an output OUT1 of the flip-flop changes (see slanted lines in FIG. 2D).

Claims 1-11 and 25 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,128,974 to Maekawa in view of U.S. Patent 5,602,561 to Kawaguchi et al. (hereinafter "Kawaguchi"). Claims 12-24 were rejected under 35 USC 103(a) as being unpatentable over Maekawa in view of Kawaguchi, and further in view of U.S. Patent 5,572,211 to Erhart et al. These rejections are respectfully traversed.

The Maekawa and Kawaguchi references, whether taken alone or in combination, do not teach or suggest a shift register circuit in which a transfer gate of a corresponding register block is brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes.

The Maekawa reference was explained in detail in Applicants' response of December 30, 2003, which is incorporated by reference herein. In Maekawa, the signal VOR_1 serves as an input to the transfer gates SW_1 and SW_2 – when VOR_1 is high, the transfer gates SW_1 and SW_2 are ON (see time period T in FIG. 8) (see also column 4, lines 49-55). The output OUT_1 represents an output of the unit register SR_1 (see column 4, lines 32-35).

It is apparent from FIG. 8 that the transfer gates SW_1 and SW_2 (see VOR_1) are turned ON at t_1 and remain ON until t_4. The output OUT_1 of unit register SR_1 is high between t_2 and t_4. Therefore, the transfer gates SW_1 and SW_2 are not brought into an ON-state only when an output OUT1 of the "flip-flop" changes. Instead, the transfer gates SW_1 and SW_2 are turned at a time t_1, which is **before** the time t_2 that the output OUT1 of the "flip flop" becomes high. Therefore, Maekawa does not teach or suggest the Applicants' claimed invention.

In the Response to Arguments section of the Final Office Action (page 9), the Examiner stated:

> Up until the period (t2) the output of the flip-flop (OUT1) is in a low state and the transfer gates are [turned] off (column 4, lines 42-48), but when the output of the flip-flop is in a high state the transfer gates are turned on (see column 4, lines 52-60)."

However, in Maekawa, the transfer gates SW_1 and SW_2 are turned on **before** OUT1 becomes high.

As shown in FIG. 8 of Maekawa, VOR_1 represents an input to the transfer gates, and VOR_1 becomes high at time t_1 (see column 4, lines 52-55: "The output and an inverted High level output VOR_1 ... are supplied to the transfer gates SW_1 and SW_2, turning both gates on.") As specified in column 4, line 50, this change in VOR_1 occurs at time t_1, but the output OUT_1 does not change until time t_2.

Therefore, it is apparent that the transfer gates SW_1 and SW_2 are turned ON (represented by signal VOR_1) at time t_1, which occurs **before** the output OUT_1 changes at time t_2. Therefore, Maekawa does not teach or suggest that a transfer gate of a corresponding register block is brought into an ON-state only in a specified period during which an output of the flip-flop of the corresponding register block changes.

Claims 3-24 incorporate the subject matter of claim 1, and thus are patentable over the cited combination of references, for at least the reasons discussed above.

It is believed that the claims are in condition for immediate allowance, which action is earnestly solicited.

Applicants believe that additional fees are not required for consideration of the within response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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